**Enrollment No: _____ Exam Seat No:_____**

# C.U.SHAH UNIVERSITY

## Summer Examination-2018

**Subject Name: Hardware Descriptive Language**

**Subject Code: 5TE01HDL1 Branch: M.Tech (VESD)**

**Semester: 1 Date: 21/03/2018 Time: 02:30 To 05:30 Marks: 70**

**Instructions:**

(1) Use of Programmable calculator and any other electronic instrument is prohibited.
(2) Instructions written on main answer book are strictly to be obeyed.
(3) Draw neat diagrams and figures (if necessary) at right places.
(4) Assume suitable data if needed.

---

## SECTION – I

**Q-1** **Attempt the following questions:** **(07)**

**a.** Verilog HDL was first developed by which company?
**b.** What are the two main data types in Verilog HDL?
**c.** In which year was Verilog HDL first standardized by the IEEE?
**d.** What does UDP stand for?
**e.** Can a test bench be written using Verilog HDL?
**f.** Draw the diagram for mixed level modeling in Verilog HDL.
**g.** State the name of primitives used for describing structure of design in Verilog HDL.

**Q-2** **Attempt all questions** **(14)**

**(a)** Enlist operands used in Verilog HDL and explain any four in detail. **(07)**
**(b)** Explain in detail with example behavioral style design in Verilog HDL. **(07)**

**OR**

**Q-2** **Attempt all questions** **(14)**

**(a)** Enlist operators used in Verilog HDL and explain any four in detail. **(07)**
**(b)** Explain in detail with example mixed-design style in Verilog HDL. **(07)**

**Q-3** **Attempt all questions** **(14)**

**(a)** Write a model, in structural style, for the 1-bit full adder. **(07)**
**(b)** State and explain different net data types available in Verilog HDL. **(07)**

**OR**

**Q-3** **Attempt all questions** **(14)**

**(a)** Write a model, in structural style, for the 1-bit full subtractor. **(07)**
**(b)** State and explain in brief built in primitive gates available in Verilog HDL. **(07)**

## SECTION – II

**Q-4** **Define the following terms** **(07)**

**a.** State different kinds of behavior which can be described in UDP.
**b.** State different kinds of sequential UDP
**c.** Write syntax of case statement.
**d.** What do you mean by intra – statement delay?
**e.** What do you mean by block statement?
**f.** What do you mean by sequential block?
**g.** What do you mean by parallel block?

**Q-5** **Attempt all questions** **(14)**

**(a)** Model the 2-to-4 decoder circuit using built in primitive gates. **(07)**
**(b)** Model the 9-bit parity circuit using built in primitive gates. **(07)**

**OR**

**Q-5** **Attempt all questions** **(14)**

**(a)** Model the master slave flip flop circuit using built in primitive gates. **(07)**
**(b)** Model the 4-to-1 multiplexer circuit using built in primitive gates. **(07)**

**Q-6** **Attempt all questions** **(14)**

**(a)** Explain in detail with example combinational UDP **(07)**
**(b)** Explain in detail 2-to-4 decoder with its test bench. **(07)**

**OR**

**Q-6** **Attempt all Questions** **(14)**

**(a)** Explain in detail with example sequential UDP. **(07)**
**(b)** What do you mean by synthesis in Verilog HDL? Explain in detail synthesis in design process. **(07)**